Vlsi Physical Design From Graph Partitioning To Timing Closure

This text discusses the design and use of practical parallel algorithms for solving problems in a growing application area whose computational requirements are enormous - VLSI CAD applications.

The last decade has brought explosive growth in the technology for manufac turing integrated circuits. Integrated circuits with several hundred thousand transistors are now commonplace. This manufacturing capability, combined with the economic benefits of large electronic systems, is forcing a revolution in the design of these systems and providing a challenge to those people in terested in integrated system design. Modern circuits are too complex for an individual to comprehend completely. Managing tremendous complexity and automating the design process have become crucial issues. Two groups are interested in dealing with complexity and in developing algorithms to automate the design process. One group is composed of practi tioners in computer-aided design (CAD) who develop computer programs to aid the circuit-design process. The second group is made up of computer scientists and mathemati'::~l\ns who are interested in the design and analysis of efficient combinatorial aJ::,orithms. These two groups have developed separate bodies of literature and, until recently, have had relatively little interaction. An obstacle to bringing these two groups together is the lack of

books that discuss issues of importance to both groups in the same context. There are many instances when a familiarity with the literature of the other group would be beneficial. Some practitioners could use known theoretical results to improve their "cut and try" heuristics. In other cases, theoreticians have published impractical or highly abstracted toy formulations, thinking that the latter are important for circuit layout.

This book discusses and compares several new trends that can be used to overcome Moore's law limitations, including Neuromorphic, Approximate, Parallel, In Memory, and Quantum Computing. The author shows how these paradigms are used to enhance computing capability as developers face the practical and physical limitations of scaling, while the demand for computing power keeps increasing. The discussion includes a state-of-the-art overview and the essential details of each of these paradigms.

In the last few decades, multiscale algorithms have become a dominant trend in large-scale scientific computation. Researchers have successfully applied these methods to a wide range of simulation and optimization problems. This book gives a general overview of multiscale algorithms; applications to general combinatorial optimization problems such as graph partitioning and the traveling salesman problem; and VLSICAD applications, including circuit partitioning, placement, and VLSI routing. Additional chapters discuss optimization in reconfigurable computing, convergence in multilevel optimization, and model problems with PDE constraints. Audience: Written at the graduate level, the book is intended for

engineers and mathematical and computational scientists studying large-scale optimization in electronic design automation.

Market_Desc: · Electrical Engineering Students taking courses on VLSI systems, CAD tools for VLSI, Design Automation at Final Year or Graduate Level, Computer Science courses on the same topics, at a similar level· Practicing Engineers wishing to learn the state of the art in VLSI Design Automation· Designers of CAD tools for chip design in software houses or large electronics companies. Special Features: · Probably the first book on Design Automation for VLSI Systems which covers all stages of design from layout synthesis through logic synthesis to high-level synthesis· Clear, precise presentation of examples, well illustrated with over 200 figures· Focus on algorithms for VLSI design tools means it will appeal to some Computer Science as well as Electrical Engineering departments About The Book: Enrollments in VLSI design automation courses are not large but it's a very popular elective, especially for those seeking a career in the microelectronics industry. Already the reviewers seem very enthusiastic about the coverage of the book being a better match for their courses than available competitors, because it covers all design phases. It has plenty of worked problems and a large no. of illustrations. It's a good 'list-builder' title that matches our strategy of focusing on topics that lie on the interface between Elec Eng and Computer Science.

Proceedings of a workshop which aims to integrate theory and applications, and to find out mechanisms, concepts or tools which facilitate the implementation of solutions based on graphs. Numerous applications are covered.

During the last few years, computers have evolved from pure number crunching machines to "intelligent" problem solving tools. Increasing effort has been spent on the investigation of new approaches and the application of solutions to real world problems. In this way, exciting new techniques have evolved providing support for an increasing number of technical and economical aspects. Applications range from the design and development of ultra highly integrated circuits to totally new man-machine interfaces, from software engineering tools to fault diagnosis systems, from decision support to even the analysis of unemployment. Following a first joint workshop on Advanced Information Processing held in July 1988 at the Institute for Problems of Informatics of the USSR Academy of Sciences (IPIAN) at Moscow, this was the second time that scientists and researchers from the USSR Academy of Sciences and Siemens AG, Corporate Research and Development, exchanged results and discussed recent advances in the field of applied computer sciences. Initiated by Prof. Dr. I. Mizin, Corresponding Member of the USSR Academy of Sciences and Director of IPIAN, and Prof. Dr. H. Schwartzel, Vice President of the Siemens AG and Head of the Applied Computer Science & Software Department, a joint symposium was arranged at the USSR Academy of Sciences in Moscow on June 5th and 6th 1990. The meetings on Information Processing and Software and Systems Design Automation provided a basis both for presentations of ongoing research and for discussions about specific problems.

Microfluidic Very Large Scale Integration (VLSI)

The physical design flow of any project depends upon the size of the design, the technology, the number of designers, the clock frequency, and the time to do the design. As technology advances and design-styles change, physical design flows are constantly reinvented as traditional phases are removed and new ones are added to accommodate changes in technology. Handbook of Algorithms for Physical Design Automation provides a detailed overview of VLSI physical design automation, emphasizing state-of-the-art techniques, trends and improvements that

have emerged during the previous decade. After a brief introduction to the modern physical design problem, basic algorithmic techniques, and partitioning, the book discusses significant advances in floorplanning representations and describes recent formulations of the floorplanning problem. The text also addresses issues of placement, net layout and optimization, routing multiple signal nets, manufacturability, physical synthesis, special nets, and designing for specialized technologies. It includes a personal perspective from Ralph Otten as he looks back on the major technical milestones in the history of physical design automation. Although several books on this topic are currently available, most are either too broad or out of date. Alternatively, proceedings and journal articles are valuable resources for researchers in this area, but the material is widely dispersed in the literature. This handbook pulls together a broad variety of perspectives on the most challenging problems in the field, and focuses on emerging problems and research results.

The Complete, Modern Tutorial on Practical VLSI Chip Design, Validation, and Analysis As microelectronics engineers design complex chips using existing circuit libraries, they must ensure correct logical, physical, and electrical properties, and prepare for reliable foundry fabrication. VLSI

Design Methodology Development focuses on the design and analysis steps needed to perform these tasks and successfully complete a modern chip design. Microprocessor design authority Tom Dillinger carefully introduces core concepts, and then guides engineers through modeling, functional design validation, design implementation, electrical analysis, and release to manufacturing. Writing from the engineer's perspective, he covers underlying EDA tool algorithms, flows, criteria for assessing project status, and key tradeoffs and interdependencies. This fresh and accessible tutorial will be valuable to all VLSI system designers, senior undergraduate or graduate students of microelectronics design, and companies offering internal courses for engineers at all levels. Reflect complexity, cost, resources, and schedules in planning a chip design project Perform hierarchical design decomposition, floorplanning, and physical integration, addressing DFT, DFM, and DFY requirements Model functionality and behavior, validate designs, and verify formal equivalency Apply EDA tools for logic synthesis, placement, and routing Analyze timing, noise, power, and electrical issues Prepare for manufacturing release and bring-up, from mastering ECOs to qualification This guide is for all VLSI system designers, senior undergraduate or graduate students of microelectronics

design, and companies offering internal courses for engineers at all levels. It is applicable to engineering teams undertaking new projects and migrating existing designs to new technologies.

This book is intended to gather recent studies on particle swarm optimization (PSO). In this book, readers can find the recent theoretical developments and applications on PSO algorithm. From the theoretical aspect, PSO has preserved its popularity because of the fast convergence rate, and a lot of hybrid algorithms have recently been developed in order to increase the performance of the algorithm. At the same time, PSO has also been used to solve different kinds of engineering optimization problems. In this book, a reader can find engineering applications of PSO, such as environmental economic dispatch and grid computing.

Discrete mathematics and theoretical computer science are closely linked research areas with strong impacts on applications and various other scientific disciplines. Both fields deeply cross fertilize each other. One of the persons who particularly contributed to building bridges between these and many other areas is László Lovász, a scholar whose outstanding scientific work has defined and shaped many research directions in the last 40 years. A number of friends and colleagues, all top authorities in their

fields of expertise and all invited plenary speakers at one of two conferences in August 2008 in Hungary, both celebrating Lovász's 60th birthday, have contributed their latest research papers to this volume. This collection of articles offers an excellent view on the state of combinatorics and related topics and will be of interest for experienced specialists as well as young researchers.

This book constitutes the refereed proceedings of the 8th International Conference on Artificial Intelligence and Soft Computing, ICAISC 2006, held in Zakopane, Poland, in June 2006. The 128 revised contributed papers presented are organized in topical sections on neural networks and their applications, fuzzy systems and their applications, evolutionary algorithms and their applications, rough sets, classification and clustering, image analysis and robotics, bioinformatics and medical applications, various problems of artificial intelligence.

One of the main problems in chip design is the enormous number of possible combinations of individual chip elements within a system, and the problem of their compatibility. The recent application of data structures, efficient algorithms, and ordered binary decision diagrams (OBDDs) has proven vital in designing the computer chips of tomorrow. This book

provides an introduction to the foundations of this interdisciplinary research area, emphasizing its applications in computer aided circuit design.

&Quot;VLSI Physical Design Automation: Theory and Practice is an essential introduction for senior undergraduates, postgraduates and anyone starting work in the field of CAD for VLSI. It covers all aspects of physical design, together with such related areas as automatic cell generation, silicon compilation, layout editors and compaction. A problem-solving approach is adopted and each solution is illustrated with examples. Each topic is treated in a standard format: Problem Definition, Cost Functions and Constraints, Possible Approaches and Latest Developments."--BOOK JACKET.

A Comprehensive Guide

RTL Design Using Verilog

Modeling, Simulation, Testing, Compilation and Physical Synthesis

Static Timing Analysis for Nanometer Designs

Parallel Methods for VLSI Layout Design

VLSI Design and EDA Tools

Advanced Information Processing

Algorithms for VLSI Physical Design Automation
Practical Problems in VLSI Physical Design Automation
OBDD - Foundations and Applications
CMOS VLSI Design: A Circuits and Systems Perspective

This book provides a single-source reference to the state-of-the-art in logic synthesis. Readers will benefit from the authors' expert perspectives on new technologies and logic synthesis, new data structures, big data and logic synthesis, and convergent logic synthesis. The authors describe techniques that will enable readers to take advantage of recent advances in big data techniques and frameworks in order to have better logic synthesis algorithms.
This book provides readers with an up-to-date account of the use of machine learning frameworks, methodologies, algorithms and techniques in the context of computer-aided design (CAD) for very-large-scale integrated circuits (VLSI). Coverage includes the various machine learning methods used in lithography, physical design, yield prediction, post-silicon performance analysis, reliability and failure analysis, power and thermal analysis, analog design, logic synthesis, verification, and neuromorphic design. Provides up-to-date information on machine learning in VLSI CAD for device modeling, layout verifications, yield prediction, post-silicon validation, and

reliability; Discusses the use of machine learning techniques in the context of analog and digital synthesis; Demonstrates how to formulate VLSI CAD objectives as machine learning problems and provides a comprehensive treatment of their efficient solutions; Discusses the tradeoff between the cost of collecting data and prediction accuracy and provides a methodology for using prior data to reduce cost of data collection in the design, testing and validation of both analog and digital VLSI designs. From the Foreword As the semiconductor industry embraces the rising swell of cognitive systems and edge intelligence, this book could serve as a harbinger and example of the osmosis that will exist between our cognitive structures and methods, on the one hand, and the hardware architectures and technologies that will support them, on the other....As we transition from the computing era to the cognitive one, it behooves us to remember the success story of VLSI CAD and to earnestly seek the help of the invisible hand so that our future cognitive systems are used to design more powerful cognitive systems. This book is very much aligned with this on-going transition from computing to cognition, and it is with deep pleasure that I recommend it to all those who are actively engaged in this exciting transformation. Dr. Ruchir Puri, IBM Fellow, IBM Watson CTO & Chief Architect, IBM T. J. Watson Research Center

This book presents the state-of-the-art techniques for the modeling,

simulation, testing, compilation and physical synthesis of mVLSI biochips. The authors describe a top-down modeling and synthesis methodology for the mVLSI biochips, inspired by microelectronics VLSI methodologies. They introduce a modeling framework for the components and the biochip architecture, and a high-level microfluidic protocol language. Coverage includes a topology graph-based model for the biochip architecture, and a sequencing graph to model for biochemical application, showing how the application model can be obtained from the protocol language. The techniques described facilitate programmability and automation, enabling developers in the emerging, large biochip market.

Design and optimization of integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. VLSI Physical Design: From

Graph Partitioning to Timing Closure introduces and compares algorithms that are used during the physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

This book provides broad and comprehensive coverage of the entire EDA flow. EDA/VLSI practitioners and researchers in need of fluency in an "adjacent" field will find this an invaluable reference to the basic EDA concepts, principles, data structures, algorithms, and architectures for the design, verification, and test of VLSI circuits. Anyone who needs to learn the concepts, principles, data structures, algorithms, and architectures of the EDA flow will benefit from this book. Covers complete spectrum of the EDA flow, from ESL design modeling to logic/test synthesis, verification, physical design, and test - helps EDA newcomers to get "up-and-running" quickly Includes comprehensive coverage of EDA concepts, principles, data structures, algorithms, and architectures - helps all readers improve their VLSI design competence Contains latest advancements not yet available in other books, including Test compression, ESL design modeling, large-scale floorplanning, placement, routing, synthesis of clock and power/ground networks - helps readers to design/develop testable chips

or products Includes industry best-practices wherever appropriate in most chapters - helps readers avoid costly mistakes

Algorithms for VLSI Physical Design Automation is a core reference text for graduate students and CAD professionals. It provides a comprehensive treatment of the principles and algorithms of VLSI physical design. Algorithms for VLSI Physical Design Automation presents the concepts and algorithms in an intuitive manner. Each chapter contains 3-4 algorithms that are discussed in detail. Additional algorithms are presented in a somewhat shorter format. References to advanced algorithms are presented at the end of each chapter. Algorithms for VLSI Physical Design Automation covers all aspects of physical design. The first three chapters provide the background material while the subsequent chapters focus on each phase of the physical design cycle. In addition, newer topics like physical design automation of FPGAs and MCMs have been included. The author provides an extensive bibliography which is useful for finding advanced material on a topic. Algorithms for VLSI Physical Design Automation is an invaluable reference for professionals in layout, design automation and physical design.

This book originated from a workshop held at the DATE 2005 conference, namely Designing Complex SOCs. State-of-the-art in issues related to System-on-Chip (SoC) design by leading experts in the fields, it

covers IP development, verification, integration, chip implementation, testing and software. It contains valuable academic and industrial examples for those involved with the design of complex SOCs.

An Introduction to VLSI Physical Design

ALGORITHMS VLSI DESIGN AUTOMATION

Advances in Evolutionary Computing

Parallel, Approximation, Near Memory, and Quantum

VLSI Physical Design: From Graph Partitioning to Timing Closure

8th International Conference, Zakopane, Poland, June 25-29, 2006, Proceedings

Synthesis & Optimizatn Of Dig. Circuits

Algorithmic Aspects of VLSI Layout

Parallel Algorithms for VLSI Computer-aided Design

Neuromorphic Computing and Beyond

Designing Complex Systems-on-Chip

This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing

and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.
The book provides a comprehensive overview of electromigration and its effects on the reliability of electronic circuits. It introduces the physical process of electromigration, which gives the reader the requisite understanding and knowledge for adopting appropriate counter measures. A comprehensive set of options is presented for modifying the present IC design methodology to prevent electromigration. Finally, the authors show how specific effects can be exploited in present and future technologies to reduce electromigration's negative impact on circuit reliability.
Arranged in a format that follows the industry-common ASIC physical design flow, Physical Design Essentials begins with general concepts of an ASIC library, then examines floorplanning, placement, routing, verification, and finally, testing. Among the topics covered are Basic standard cell design, transistor-sizing, and layout styles; Linear, non-linear, and polynomial characterization; Physical design constraints and floorplanning styles; Algorithms used for placement; Clock Tree Synthesis; Parasitic extraction; Electronic Testing, and many more.
Practical Problems in VLSI Physical Design Automation contains problems and solutions related to various well-known algorithms used in VLSI physical design automation. Dr. Lim

believes that the best way to learn new algorithms is to walk through a small example by hand. This knowledge will greatly help understand, analyze, and improve some of the well-known algorithms. The author has designed and taught a graduate-level course on physical CAD for VLSI at Georgia Tech. Over the years he has written his homework with such a focus and has maintained typeset version of the solutions.

In the past two decades, research in VLSI physical design has been directed toward automation of layout process. Since the cost of fabricating a circuit is a fast growing function of the circuit area, circuit layout techniques are developed with an aim to produce layouts with small areas. Other criteria of optimality such as delay and via minimization need to be taken into consideration. This book includes 14 articles that deal with various stages of the VLSI layout problem. It covers topics including partitioning, floorplanning, placement, global routing, detailed routing and layout verification. Some of the chapters are review articles, giving the state-of-the-art of the problems related to timing driven placement, global and detailed routing, and circuit partitioning. The rest of the book contains research articles, giving recent findings of new approaches to the above-mentioned problems. They are all written by leading experts in the field. This book will serve as good references for both researchers and professionals who work in this field. Contents:Issues in Timing Driven Layout (M Marek-Sadowska)Binary Formulations for Placement and Routing Problems (S M Kang & M Sriram)A Survey of Parallel Algorithms for VLSI Cell Placement (P Banerjee)Approximate Solutions for Graph and Hypergraph Partitioning (F Makedon & S Tragoudas)Integer Program Formulations of Global

Routing and Placement Problems (T Lengauer and M Lügering)Circuit Partitioning Algorithms Based on Geometry Model (T Asano & T Tokuyama)The Three-Dimensional Channel Routing Problem (M L Brady et al.)On the Manhattan and Knock-Knee Routing Models (D Zhou & F P Preparata)Switch-Box Routing Under the Two-Overlap Wiring Model (T F Gonzalez et al.)A Note on the Complexity of Stockmeyer's Floorplan Optimization Technique (T-C Wang & D F Wong)An Algorithm to Eliminate All Complex Triangles in a Maximal Planar Graph for Use in VLSI Floorplan (S Tsukiyama et al.)Constrained Via Minimization and Signed Hypergraph Partitioning (C-J Shi)The Virtual Dimensions of a Straight Line Embedding of a Plane Graph (T Takahashi & Y Kajitani)Routing Around Two Rectangles to Minimize the Layout Area (T F Gonzalez & S L Lee) Readership: Computer scientists. keywords:

This book provides a comprehensive overview of the VLSI design process. It covers end-to-end system on chip (SoC) design, including design methodology, the design environment, tools, choice of design components, handoff procedures, and design infrastructure needs. The book also offers critical guidance on the latest UPF-based low power design flow issues for deep submicron SOC designs, which will prepare readers for the challenges of working at the nanotechnology scale. This practical guide will provide engineers who aspire to be VLSI designers with the techniques and tools of the trade, and will also be a valuable professional reference for those already working in VLSI design and verification with a focus on complex SoC designs. A comprehensive practical guide for VLSI designers; Covers end-to-end VLSI SoC design flow; Includes source code, case studies, and application examples.

Design and optimization of integrated circuits are essential to the creation of new semiconductor chips, and physical optimizations are becoming more prominent as a result of semiconductor scaling. Modern chip design has become so complex that it is largely performed by specialized software, which is frequently updated to address advances in semiconductor technologies and increased problem complexities. A user of such software needs a high-level understanding of the underlying mathematical models and algorithms. On the other hand, a developer of such software must have a keen understanding of computer science aspects, including algorithmic performance bottlenecks and how various algorithms operate and interact. "VLSI Physical Design: From Graph Partitioning to Timing Closure" introduces and compares algorithms that are used during the physical design phase of integrated-circuit design, wherein a geometric chip layout is produced starting from an abstract circuit design. The emphasis is on essential and fundamental techniques, ranging from hypergraph partitioning and circuit placement to timing closure.

Theory and Practice

Genetic Algorithms: For Vlsi Design, Layout & Test Automation

Graph-Theoretic Concepts in Computer Science

Handbook of Algorithms for Physical Design Automation

Between Mathematics and Computer Science

Algorithmic Graph Theory

Artificial Intelligence and Soft Computing – ICAISC 2006

Physical Design Essentials

VLSI Physical Design Automation

15th International Workshop WG '89, Castle Rolduc, The Netherlands, June 14-16, 1989, Proceedings

On Optimal Interconnections for VLSI

On Optimal Interconnections for VLSI describes, from a geometric perspective, algorithms for high-performance, high-density interconnections during the global and detailed routing phases of circuit layout. First, the book addresses area minimization, with a focus on near-optimal approximation algorithms for minimum-cost Steiner routing. In addition to practical implementations of recent methods, the implications of recent results on spanning tree degree bounds and the method of Zelikovsky are discussed. Second, the book addresses delay minimization, starting with a discussion of accurate, yet algorithmically tractable, delay models. Recent minimum-delay constructions are highlighted, including provably good cost-radius tradeoffs, critical-sink routing algorithms, Elmore delay-optimal routing, graph Steiner arborescences, non-tree routing, and wiresizing. Third, the book addresses skew minimization for clock routing and prescribed-delay routing formulations. The discussion starts with early matching-based constructions and goes on to treat zero-

skew routing with provably minimum wirelength, as well as planar clock routing. Finally, the book concludes with a discussion of multiple (competing) objectives, i.e., how to optimize area, delay, skew, and other objectives simultaneously. These techniques are useful when the routing instance has heterogeneous resources or is highly congested, as in FPGA routing, multi-chip packaging, and very dense layouts. Throughout the book, the emphasis is on practical algorithms and a complete self-contained development. On Optimal Interconnections for VLSI will be of use to both circuit designers (CAD tool users) as well as researchers and developers in the area of performance-driven physical design.

This book provides a collection of fourty articles containing new material on both theoretical aspects of Evolutionary Computing (EC), and demonstrating the usefulness/success of it for various kinds of large-scale real world problems. Around 23 articles deal with various theoretical aspects of EC and 17 articles demonstrate the success of EC methodologies. These articles are written by leading experts of the field from different countries all over the world.

Genetic Algorithms mimic the natural process of evolution, helping engineers optimize their designs by using the principle of "survival of the fittest". VLSI is especially suited to benefit from genetic algorithms- and

this comprehensive book shows how to get the best results. You will discover how genetic algorithms work and how you can use them in a wide variety of VLSI design, layout and test automation tasks.

iming, timing, timing! That is the main concern of a digital designer charged with designing a semiconductor chip. What is it, how is it T described, and how does one verify it? The design team of a large digital design may spend months architecting and iterating the design to achieve the required timing target. Besides functional verification, the t- ing closure is the major milestone which dictates when a chip can be - leased to the semiconductor foundry for fabrication. This book addresses the timing verification using static timing analysis for nanometer designs. The book has originated from many years of our working in the area of timing verification for complex nanometer designs. We have come across many design engineers trying to learn the background and various aspects of static timing analysis. Unfortunately, there is no book currently ava- able that can be used by a working engineer to get acquainted with the - tails of static timing analysis. The chip designers lack a central reference for information on timing, that covers the basics to the advanced timing veri- cation procedures and techniques.

Managing the power consumption of circuits and systems is now

considered one of the most important challenges for the semiconductor industry. Elaborate power management strategies, such as dynamic voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This book explores existing solutions for power-aware test and design-for-test of conventional circuits and systems, and surveys test strategies and EDA solutions for testing low power devices.

Power-Aware Testing and Test Strategies for Low Power Devices
Electronic Design Automation
Multilevel Optimization in VLSICAD
Algorithms and Data Structures in VLSI Design
Synthesis, Verification, and Test
Advanced Logic Synthesis
A Practical Approach to VLSI System on Chip (SoC) Design
An ASIC Design Implementation Perspective
Combinatorial Algorithms for Integrated Circuit Layout
Advanced HDL Synthesis and SOC Prototyping